Laser Testing of CULPRiT RS Encoder and USES Compression Chips

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Introduction:

There is currently much interest in the use of advanced CMOS microelectronics in the space radiation environment. Such applications can impose severe constraints on the microelectronics with regard to power consumption and radiation tolerance. In order to help meet these constraints, the NASA ST-5 mission will be utilizing RS Encoder and USES data compression chips fabricated in technology referred to as **C**MOS **U**ltra-**L**ow **P**ower **R**adiation **T**olerant (**CULPRiT**). This is a 0.5 V bulk CMOS technology that uses aggressive scaling of the supply voltage and the transistor threshold voltages to minimize the power consumption of circuits with high activity levels. For further information about CULPRiT, see reference 1. Since this is a relatively new technology for space applications, laser testing for single event effects (SEE) was performed prior to heavy ion tests that will be done at Brookhaven National Laboratory (BNL). The purpose of the laser tests was to determine first order SEE levels and to verify test setup operation before proceeding with tests at BNL.

Methods and Results:

Laser Testing. The testing was done at NRL's SEE Pulsed Laser Facility. The laser is used to generate concentrations of electron-hole pairs in semiconductors that can sometimes simulate effects caused by heavy ions. One of its advantages is its convenience. Data can be taken much more quickly than in a typical heavy ion experiment. Another advantage is that the laser light can be focused down to a beam spot close to 1 micrometer so that portions of the circuit can be tested for SEE vulnerability. One disadvantage is that the laser light can not penetrate metal layers in the chip. Another is that for bulk CMOS circuits, the penetration depth of the light is usually less than the depth from which electron-hole pairs can be collected. More details about laser testing can be found elsewhere [2].

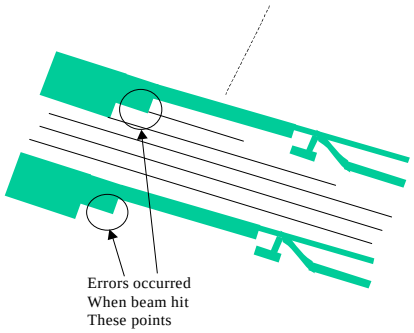
Test Boards. The RS Encoder testboard was an improved version of Mark Frigaard's RS Encoder test board that was developed within code 561. The new design utilizes a simple UART interface for testboard configuration and control and contains a Xilinx FPGA that exercises the RS Encoder and signals device health (miscompare errors and proper operation). The USES testboard was adapted from an RS Encoder testboard design from the Institute of Advanced Microelectronics (IAM) at the University of New Mexico. This design relies on an HP 16702 Logic Analyzer with a Pattern Generator plug-in to inject input data and capture output results. This setup requires more user involvement in determining error occurrence and proper operation.

RS Encoder Testing. The RS Encoder was tested first. Power supply voltage was initially set at 0.5VDC for UVDD, 1.9V (wrt GND) for positive bias, and –1.4V for negative bias. Test vector pattern was a pattern known as 2Normal_Rand2 which is described as a normal return link mode test with 8 223-byte blocks interleaved. Test frequency was 10MHz. The device was scanned over areas identified by a map of the die provided by IAM. This map was helpful because it helped economize the testing given the fine pitch of the laser beam and the large die area to cover. For example, the main area of the die comprises four similar blocks (labeled A-D) where each block is described as eight 8-bit variable length shift registers. For this test, only block D was scanned. The laser was fitted with an optical filter characterized as OD1 which corresponds to an optical density filter of 10^1. A beam splitter is inserted in the beam to direct a small fraction (~5%) of the light onto a fast photodiode. The amount of light at the DUT can be continuously monitored by first placing the photodiode at the DUT location and then at its normal location and taking the ratio of the measured light intensities. The maximum laser intensity measured by the photodiode at its normal location is determined by measuring the amplitude of output pulse generated

by the photodiode. The amplitude is proportional to the laser intensity and has a maximum value of 16.5mV. Previous experiments have shown this voltage level corresponds approximately to a heavy ion linear energy transfer (LET) of 92MeV*cm^2/mg. It is assumed that laser intensities corresponding to levels below 16.5mV can be scaled proportionally to this LET. The use of the laser system allowed the SEU-sensitive region of the chip to be located. The following results were obtained:

Area	Description	Result
M	Bias Generator	No miscompare errors at max intensity
N	Clock Input Driver Pad	same
F	Galois Field Comb. Logic	same
H	Decode Comb. Logic	same
J	Gate Caps	No errors, but metallization is a factor
D	8-bit shift registers	Miscompare errors seen at 7mV (corresponds to ~40MeV*cm^2/mg)

Area D showed consistent errors at certain repeatable spots. Pictures were taken (though no electronic copy obtained). An illustration of the susceptible area in area D is shown:



Shift register area in RS Encoder die
Susceptible to NRL laser

The structures shown in the illustration occur throughout region D on the die map.

Since the CULPRiT RS Encoders operate for a range of p-channel and n-channel back-biases, the dependence of the SEU sensitivity on these biases was measured. The encoder performance is also back-bias dependent so it is hoped that this will give the ST-5 mission the ability to trade off encoder performance vs. SEU tolerance in selecting the operating back-biases for the mission. The following results were obtained for threshold laser intensity and approximate threshold LET for observing SEU. It is noted that for both biases, the threshold LET increases with increasing bias magnitude.

+Bias	-Bias	Approx laser intensity	Corresponding LET ($MeV*cm^2/mg$)
1.9	1.4	7mV	40
2.1	1.4	7.5mV	43
2.3	1.4	8mV	44.6
2.5	1.4	9mV	52
2.7	1.4	9mV	52
2.9	1.4	9mV	52
1.7	1.4	7mV	40
1.5	1.4	6mV	33
1.3	1.4	6mV	33
1.1	1.4	6mV	33
1.9	1.2	6mV	33
1.9	1.0	4.5mV	25
1.9	0.8	4.5mV	25
1.9	1.6	8.5mV	47.4
1.9	1.8	11.5mV	64
1.9	**2.0**	**16.5mV**	**92**
1.9	**2.2**	**16.5mV**	**92**

As seen in the above data, the best combination based on the bias supply settings appears to be +/-2V. The above LET values should be regarded as approximate due to limitations in the laser testing.

USES testing. Power supply voltage was initially set at 0.5VDC for UVDD, 1.9V (wrt GND) for positive bias, and –1.4V for negative bias. Test vector pattern was an MRC-supplied pattern and test frequency was 2MHz. Testing of the USES was more difficult because there was no die map available. The test approach was to set the laser to a wider beam and to scan the laser over all parts of the die. Occasional compare errors were seen. However, consistent errors were never seen when the beam was isolated over the suspected areas. The optical filter was changed to an OD0 and the intensity level set to maximum. This level corresponds to SEU levels between 100 and 200$MeV*cm^2/mg$. As a last test, the bias voltages were reduced to try and reduce the SEU tolerance as per the trend for the RS Encoder. However, three different settings resulted in a degradation of UVDD (to <0.4V) and a significant increase in current consumption. Testing was stopped with no further conclusions on the errors.

The USES test was beneficial in that it revealed the need for some test setup improvements before going to BNL – specifically the need for easy indicators (like LEDs) of errors and proper operation. One issue that needs further investigation is power supply voltage. Pre-NRL tests showed that the UVDD supply would supply 0.5V when set to 0.5V. During NRL tests, UVDD on the board measured <0.5V. This required that the supply had to be increased to 0.56V in order to yield 0.493V on the board. In fact, UVDD on the board still dropped to as low as 0.476V during testing. One pre-NRL observation was that if insufficient bias voltage was supplied, device current would increase significantly and UVDD would drop. This possibly points to a difference in bias voltage needs between the RS Encoder and USES.

[1] M.A. Xapsos, G.P. Summers and E.M. Jackson, “Enhanced Total Ionizing Dose Tolerance of Bulk CMOS Transistors Fabricated for Ultra-Low Power Applications”, IEEE Trans. Nucl. Sci. **46**, pg. 1697-1701 (Dec. 1999), and references therein.

[2] S. Buchner, L. Tran, J. Mann, T. Turflinger, D. McMorrow, A. Campbell and C. Dozier, “Single-Event Effects in Resolver-to-Digital Converters”, IEEE Trans. Nucl. Sci. **46**, 1445-1452 (Dec. 1999).